

Claims:

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1. A semiconductor memory element, comprising:
a source region,
a drain region,
a channel region made of a semiconductor,
the source region and the drain region being
connected by the channel region,

a gate electrode made of a metal or a
semiconductor for controlling the electric potential of
the channel region, and

a plurality of charge storage regions in the
vicinity of the channel region,

the electric potential to be applied to the gate
electrode upon writing of data and the electric
potential to be applied to the gate electrode upon
erasing of data having the same polarity.

2. A semiconductor memory element, comprising:
a channel region made of a semiconductor, the
channel region including a first channel region which
is a part of the channel region, and a second channel
region which is a part of the channel region, and
different from the first channel region,

a plurality of charge storage regions in the
vicinity of the channel region,

a first gate electrode made of a metal or a
semiconductor for controlling the electric potential of
the first channel region, and

a second gate electrode made of a metal or a

semiconductor for controlling the electric potential of the second channel region,

the electric potential to be applied to the first gate electrode upon writing of data and the electric potential to be applied to the first gate electrode upon erasing of data having the same polarity.

3. A semiconductor memory element, comprising:

a channel region made of a semiconductor, the channel region including a first channel region which is a part of the channel region, and a second channel region which is a part of the channel region, and different from the first channel region,

a plurality of charge storage regions in the vicinity of the channel region,

a first gate electrode made of a metal or a semiconductor for controlling the electric potential of the first channel region, and

a second gate electrode made of a metal or a semiconductor for controlling the electric potential of the second channel region,

the electric potential to be applied to the first gate electrode upon writing of data and the electric potential to be applied to the second gate electrode upon erasing of data having the same polarity.

4. A semiconductor memory element, comprising:

a source region,

a drain region,

a channel region made of a semiconductor, the

channel region including a first channel region which is a part of the channel region, and a second channel region which is a part of the channel region, and different from the first channel region,

5 the source region and the drain region being connected by the channel region,

a1 a plurality of charge storage regions in the vicinity of the channel region,

10 a first gate electrode made of a metal or a semiconductor for controlling the electric potential of the first channel region, and

a second gate electrode made of a metal or a semiconductor for controlling the electric potential of the second channel region,

15 the electric potential to be applied to the first gate electrode upon writing of data and the electric potential to be applied to the first gate electrode upon erasing of data having the same polarity.

5. A semiconductor memory element, comprising:

20 a source region,

a drain region,

a channel region made of a semiconductor, the channel region including a first channel region which is a part of the channel region, and a second channel region which is a part of the channel region, and different from the first channel region,

25 the source region and the drain region being connected by the channel region,

a plurality of charge storage regions in the vicinity of the channel region,

a first gate electrode made of a metal or a semiconductor for controlling the electric potential of the first channel region, and

a second gate electrode made of a metal or a semiconductor for controlling the electric potential of the second channel region,

the electric potential to be applied to the first gate electrode upon writing of data and the electric potential to be applied to the second gate electrode upon erasing of data having the same polarity.

6. A semiconductor memory device, comprising:

a memory cell array comprising a plurality of semiconductor memory elements, each comprising:

a source region,

a drain region,

a channel region made of a semiconductor, the channel region including a first channel region which is a part of the channel region, and a second channel region which is a part of the channel region, and different from the first channel region,

the source region and the drain region being connected by the channel region,

a plurality of charge storage regions in the vicinity of the channel region,

a first gate electrode made of a metal or a semiconductor for controlling the electric potential of

the first channel region, and

a second gate electrode made of a metal or a semiconductor for controlling the electric potential of the second channel region,

5 the plurality of the semiconductor memory elements being arranged in an array,

a data line,

a first word line, and

a second word line,

10 the memory cell array being driven by the data line, the first word line, and the second word line,

the drain regions of the plurality of the semiconductor memory elements being connected to the same data line,

15 the second gate electrodes of the plurality of the semiconductor memory elements of which the drain regions are connected to the same data line being connected to mutually different second word lines, and

20 the first gate electrodes of the plurality of the semiconductor memory elements of which the drain regions are connected to the same data line being connected to mutually different first word lines.

7. A semiconductor memory device, comprising:

a memory cell array comprising a plurality of

25 the semiconductor memory elements according to claim 1,

the plurality of the semiconductor memory elements being arranged in an array,

a data line, and

a word line,
the memory cell array being driven by the data
line and the word line,

the drain regions of the plurality of the
5 semiconductor memory elements being connected to the
same data line, and

91
the gate electrodes of the plurality of the
semiconductor memory elements of which the drain
regions are connected to the same data line being
10 connected to mutually different word lines.

8. A semiconductor memory device, comprising:

a plurality of the semiconductor memory elements
according to any of claims 1 to 3,

the plurality of the semiconductor memory
15 elements being arranged,

a connection being established such that the
channel currents of a first semiconductor memory
element and a second semiconductor memory element flow
in series.

20 9. A semiconductor memory device, comprising:

a memory cell array comprising a plurality of
the semiconductor memory elements according to any of
claim 4 or 5, the plurality of the semiconductor memory
elements being arranged in an array,

25 a data line, and

a first word line,

the memory cell array being driven by the data
line and the first word line,

the semiconductor memory elements of which the drain regions are connected to the same data line being connected to mutually different first word lines.